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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/517,345	03/02/2000	Sidney Larry Anderson	15114-052310	4253

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/517,345	Anderson et al
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Apr 15, 2002* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-25 and 49-61* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-25 and 49-61* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *and 1*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-25 and 49-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Schueller (US Pat. 5866949) in view of Zenner et al (US Pat. 6246010), Welkowsky et al (US Pat. 5160560) and the admitted prior art (APA).

Regarding claims 1 and 18, Schueller discloses an integrated circuit (IC)/BGA package comprising:

- a silicon die (52 in Fig. 3B/3A) having a first thickness
- a metallized polymer layer (58/59/60 in Fig. 3B/3A) having a first side and a second side, and
- a transition medium/support structure (50 in Fig. 3B/3A) disposed between the silicon die and the first side of the metallized polymer layer where the transition medium/support structure has a second thickness

(Fig. 3B/3A; Col. 8, line 12- Col. 10, line 36; Col. 5, line 36- Col. 6, line 55).

Schueller discloses using a single transition medium/support structure having a second thickness of 100-250 microns (Col. 9, line 49) or using a plurality of those (Col. 11, line 12) but fails to specify the first thickness of the silicon die being less than the second thickness.

Zenner et al teach using conventional high density/thin packages having a die thickness of about less than 100 microns and a package thickness of about 275 microns (Col. 2, line 15-22).

Welkowsky et al teach using thin chips/wafers for a variety of semiconductor applications where the chip thicknesses are about 30 microns, 5 mils , etc. (Col. 7, line 20-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first thickness of the silicon die with a smaller thickness than the second thickness of transition medium so that the thermal stress can be reduced and the package flexibility can be retained using Zenner et al and Welkowsky et al's chip designs in Schueller.

Regarding claim 2, Schueller discloses the transition medium/support structure comprising a single or multilayered structure including conventional conductive/non-

conductive material such as ceramic, metal, PCB or a combination of metal and non-metal/epoxy PCB material (Col. 9, line 58; Col. 10, line 27; Col. 11, line 12).

Regarding claims 3 and 11, Schueller further discloses encapsulating the silicon die and the transition medium with a conventional plastic encapsulant/mold cap, the die being disposed near the middle of the package (Col. 8, line 40; Fig. 3B) but fails to specify the encapsulant and adhesive having a thermal coefficient of expansion (CTE) approximately in a range of 7-15 x $10^{-6}/^{0}$C and 58 x $10^{-6}/^{0}$C respectively.

The conventional encapsulant and adhesives have thermal coefficient of expansion (CTE) range of 7-15 x $10^{-6}/^{0}$C and approximately 58 x $10^{-6}/^{0}$C respectively (Table 2- admitted prior art).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plastic encapsulant having approximate CTE range of 7-17 x $10^{-6}/^{0}$C so that the thermal stress can be reduced in Schueller's package in view of Zenner et al, Welkowsky et al and APA.

Regarding claims 4 and 5, Schueller discloses the transition medium/support structure used to reduce the thermal stress/cracks and to improve the reliability and of conventional nonconductive epoxy/PCB type material (Col. 10, line 18-27) but fails to specify the range of CTE of the material.

Schueller further discloses conventional BGA packages using elastomers and adhesives as a transition medium (Fig. 2; Col. 5 and 6) to reduce the thermal stress.

It is conventional in chip packaging art to use such nonconductive material/packaging substrates as epoxy, molded plastic, FR-4/5, BT resin, etc. which have typical CTE in the range of 10-17 x $10^{-6}/^{0}C$ (see admitted prior art-Table 2).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the transition medium comprising molded compound, FR-4/5, or BT resin compound and having the CTE range of 7-17 x $10^{-6}/^{0}C$ so that the thermal stress can be reduced in Schueller's package in view of Zenner et al, Welkowsky et al and APA.

Regarding claims 6 and 7, the claim elements are addressed as explained in the above rejections for claims 1; 4; 5 and 1; 3 respectively.

Regarding claims 8, 9, 16, 17 and 19, as explained above for claim 1, Schueller fails to specify the dimensions such as the thickness of the package and die being 0.06 inches and 6 mils respectively or the cross-sectional area/volume of the die being larger/smaller than that of the transition medium respectively.

As explained above for claim 1, Zenner et al and Welkowsky et al teach using a the die and package thickness of about 30-100 microns or 5 mils and 275 microns or

0.01 inches respectively. Such parameters as the package/die thickness, area, area ratio of various components, volume, weight, etc. in the chip packaging art are a matter of design choice and are selected to achieve the desired device performance, reliability and weight/size requirements.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the thickness of the package and the die to be less than approximately 0.060 inches and 6 mils respectively and the area/volume of the die being less than, equal or larger than that of the transition medium so that the thermal stress can be reduced and the package flexibility can be retained using Zenner et al and Welkowsky et al's chip designs in Schueller.

Regarding claim 10, Schueller discloses coupling of the silicon die to the transition medium using an adhesive (Fig. 3B; Layer 64).

Regarding claims 12-15, Schueller discloses a tape carrier having a dielectric and conductive layers as IC metallized polymer layer and solder balls mounted to the second side of the metallized polymer layer, the solder balls electrically contacting the etched circuit in a conductive layer of the tape carrier and arranged in a grid fashion under the position of the die and connecting the package to a PCB (Fig. 3B; Col. 7, lines 32 and 58; Col. 5-12; Fig. 6).

Regarding claims 20-24, the claim elements are addressed as explained in the above rejections for claims 1; 3, 5, 4 and 12 respectively.

Regarding claim 25, as explained above for claim 1, Schueller further discloses using the first and second adhesive layers (56/64 in Fig. 3B) having respective thickness/CTE disposed on the tape carrier and the transition medium respectively (Fig. 3B; Col. 9, line 65; Col. 8, line 12- Col. 10, line 36) and the adhesive layers having thickness in a range of 25-50 microns (Col. 10, line 18) which is less than that of the transition medium/support which is 100-250 microns (Col. 9, line 49) but fails to specify the thickness of the adhesive, transition medium and die being nearly equivalent or same as half of the package thickness to reduce the thermal stress.

As explained above for claim 1, Zenner et al and Welkowsky et al teach using a the die thickness of about 30-100 microns or 5 mils and package thickness of about 275 microns or 0.01 inches. Such parameters as the package/die thickness, area, area ratio of various components, volume, weight, etc. in the chip packaging art are a matter of design choice and are selected to achieve the desired device performance, reliability and weight/size requirements.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the package/die dimensions such that the thickness of the adhesive, transition medium and die being nearly equivalent or same as half of the package thickness so that the thermal stress can be reduced and the package flexibility can be retained using Zenner et al and Welkowsky et al's chip designs in Schueller.

Regarding claims 49-54, 56-59 and 61, Schueller discloses an integrated circuit (IC)/Ball Grid Array (BGA) package comprising a single or multiple IC dice:

- an IC die (52 in Fig. 3A) having a front side, backside and a first thickness between the front and back sides, where the bonding pads (Col. 8, line 25) are formed on the front side
- a metallized polymer layer/tape (58/59/60 in Fig. 3A) having a first side and a second side wherein the bonding pads are electrically coupled to the features/patterns (59 in Fig. 3A) of the metallized polymer layer/tape using bonding wires (82A in Fig. 3A)
- a transition medium/support structure between the IC die and the metallized polymer layer (50A in Fig. 3A) having only an adhesive layer (64A in Fig. 3A) between the two where the transition medium/support structure has a second thickness, the second thickness being relatively uniform and none of the bonding pads being electrically coupled to the transition medium

- the backside of the IC die faces toward the transition medium and the front side of the IC die faces away from the metallized polymer layer/tape

- the IC die, metallized polymer layer/tape and transition medium are parallel planes, and

- solder balls (54 in Fig. 3A) below the metallized polymer layer/tape and the IC die electrically coupled to the bonding pads

(Fig. 3A; Col. 8, line 24; Col. 7, line 3- Col.1, line 12).

Schueller fail to specify the transition medium/support structure having the second thickness being greater than the first thickness.

As explained above for claim 1, Schueller in view of Zenner et al and Welkowsky et al teach using the second thickness being greater than the first thickness.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the transition medium/support structure having greater thickness than that of the first thickness of the die so that the thermal stress can be reduced and the package flexibility can be retained using Zenner et al and Welkowsky et al's chip designs in Schueller.

Regarding claim 55, Schueller further discloses using the transition medium/support comprising a single or multilayered structure including non-polymer material, ceramic or

a combination of metal and non-metal/epoxy PCB material (Col. 9, line 58; Col. 10, line 27; Col. 11, line 12).

Regarding claim 60, the claim elements are addressed as explained in the above rejections for claims 1 and 5.

Response to Arguments

3. Applicant's arguments with respect to claims 1-25 and 49-61 have been considered but are moot in view of the new ground(s) of rejection.

Papers related to this application may be submitted directly to Art Unit 2811 by Facsimile transmission. Papers should be faxed to Art Unit via Tech Center 2800 fax center located in Crystal Plaza 4, Room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh at (703) 305-3410. The examiner can normally be reached on Monday-Friday from 08:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

07-03-02

Steven Loke
Primary Examiner

Steven Loke